Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (cancelled).

Claim 6 (previously presented): A clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range;

a current amplifier drawing a current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range;

a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range; and

wherein said current amplifier includes:

a second transistor and a third transistor, wherein a gate terminal of said third transistor is connected to a drain terminal of said second transistor, a gate terminal of said second transistor receiving a second bias voltage, a source terminal of each of said second transistor and said third transistor is connected to ground, said drain terminal of said second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said third transistor is connected to said source terminal of said first transistor.

Claim 7 (previously presented): The clamping circuit of claim 6, wherein each of said second transistor and said third transistor comprises a NMOS transistor.

Claims 8 and 9 (cancelled).

Claim 10 (previously presented): A clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor with a source terminal connected to the said node designed to be turned on when said voltage level is outside of said specified range;

a current amplifier drawing a current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range; and

a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range,

wherein said current amplifier comprises:

a second transistor and a third transistor, wherein a gate terminal of said third transistor is connected to both drain and gate terminals of said second transistor, a source terminal of said third transistor is connected to ground, said drain terminal of said second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said third transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said second transistor and ground.

Claims 11-17 (cancelled).

Claim 18 (previously presented): A device comprising:

a clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range, wherein said clamping circuit further comprises a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range, and

wherein said current amplifier comprises:

a second transistor and a third transistor, wherein a gate terminal of said third transistor is connected to a drain terminal of said second transistor, a gate terminal of said second transistor receiving a second bias voltage, a source terminal of each of said second transistor and said third transistor is connected to ground, said drain terminal of said second transistor is connected to a drain terminal of said first transistor, and a drain terminal of said third transistor is connected to said source terminal of said first transistor.

Claim 19 (previously presented): The device of claim 18, wherein each of said second transistor and said third transistor comprises a NMOS transistor.

Claims 20 - 25 (cancelled).

Claim 26 (currently amended): The clamping circuit of claim [10] 6, wherein said circuit is contained in an ADC.

Claim 27 (currently amended): The device of claim [22] 18, wherein the clamping circuit is contained in an ADC.

Claim 28 (new): The clamping circuit of claim 6, wherein said gate terminal of said second transistor is connected to said drain terminal of said second transistor.

Claim 29 (new): The clamping circuit of claim 6, wherein said gate terminal of said second transistor is connected to said drain terminal of said second transistor; and said source terminal of said second transistor is connected to ground through a resistor.